Software development tool for PicoBlaze multi-processor implementation

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***Abstract*— This paper presents a useful software tool for projects with multi PicoBlaze microprocessors implemented in FPGA circuits. Application presented in this paper which use for software development PicoBlaze SDK tool is an Automatic Packet Report System (APRS), with three PicoBlaze microprocessors implemented in FPGA circuit.**

I. Introduction

A major improvement in digital design it can be observed in the last few years. One of this improvement it was generated by process of development in Field programmable gate arrays (FPGAs) that in present can contain over a million equivalent logic gates and more than tens of thousands of flip-flops. Digital systems are implemented like software file written in the form of hardware description languages (HDLs). The most common HDLs formats used in this moment are VHDL and Verilog. These hardware description languages allow to designer to describe the *behavior* of the logic circuit. Computer-aided design tools are widely used to *simulate* the VHDL or Verilog design and to *synthesize* the design for specific hardware chip.

The FPGA circuits come to meet the demands mentioned above, allowing an easy implementation of both the control algorithms and the auxiliary functions on a single silicon chip, at very high speeds, all operations being executed in hardware. Another advantage offered by the programmable logic circuits is development time, very short in this case [1].

More and more often we need powerful computer architectures to solve complex problems in a short period of time. From economy point of view it is less expensive to use multiple processing cores working on same project than one stand alone and high performance processor, so it is more reliable to design hardware architecture and implement algorithms in software for multiprocessor systems. Currently more and more projects are focused to implement multiple multiprocessor cores combined in a single chip. Thereby higher performance of implemented system can be achieved with lower working frequency. Multi-processor architectures, implemented in programmable circuits, are in a growing process of utilization, because of their ability to exploit programmable silicon parallelism at acceptable power-consumption.

The partitioning of a multiprocessor program over multiple cores is a good solution because the input specification is fully parallel. Despite the benefit they offer over single-processor architectures, it is still a problem how to write compact and efficient programs for multiple parallel cores.

In this paper, we propose the use a new software tool, for development of software application and program a series of small PicoBlaze microprocessors implemented in Field Programmable Gate Array circuits (FPGA).

II. Project implementation

Automatic Packet Report System or APRS, is an radio amateur based system for communications, in real time of information and immediate value in the local area. In addition, all data can be uploaded into the APRS Internet system (APRS-IS) and distributed for immediate access. The immediate visible aspect of APRS is internet map display but it has also messages, alerts, announcements and bulletins capability. APRS is an open system therefore anyone may place any information on his map, and it is distributed to all users in the local RF network or via the Internet. Any radio station that has an attached GPS is automatically tracked on map. Other features implemented in APRS are weather stations, alerts and other map-related amateur radio volunteer activities including Search and Rescue.

An APRS infrastructure includes a variety of Terminal Node Controller (TNC) equipment installed by individual Amateur Radio operators. This includes soundcards connected to radio stations, simple TNCs, and "smart" TNCs. The "smart" TNCs are able to find what has already happened with the packet and prevent redundant packet to overload the network [6].

Proposed parallel architecture which implements APRS node controller, consists of up to three PicoBlazes soft-core microcontroller, supported free by Xilinx and makes them to run a parallel algorithm. PicoBlaze microcontroller is chosen because it is compact, capable, and cost effective fully embedded 8-bit RISC microcontroller core optimized for Xilinx FPGA families – Spartan 2, Spartan 2E, Spartan 3, Spartan 3E, Spartan 6, Virtex 2 and Virtex 2-Pro. Compared to other family of microcontrollers it is extremely flexible and his basic functionality can be extended with additional FPGA logic added to its input/output ports [7,12].

PicoBlaze microcontroller supports a program up to 1024 instructions in one block memory. Requirements for larger program are typically resolved by using multiple PicoBlaze processors each with an associated memory to distribute the various system tasks[11].

Figure 1 present the hardware project structure. Each main functions of APRS node controller are assigned to one PicoBlaze microcontroller.

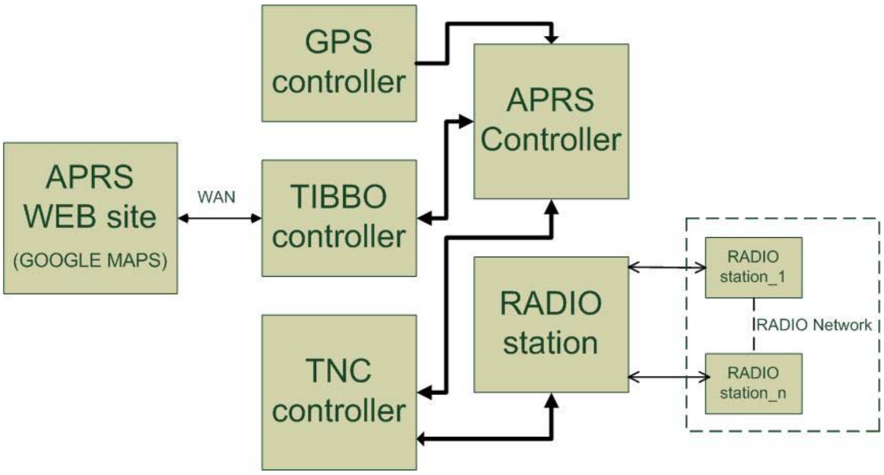


Figure 1. APRS node controller project structure

APRS node controller performs three major tasks:

1. I-Gate, internet connection function witch open Telnet session, to APRS server.
2. GPS, collect data from gps device, data needed for map placement.
3. TNC, communicate with radio interface. Communication between radio link use AFSK modulation at 1200 bauds. This radio link is used by mobile station like car, ambulance or other element from an emergency network.

Software development for all microcontrollers it was possible by using PicoBlaze SDK software, developed by authors of this paper, which allow to change program memory for all PicoBlaze microcontroller individually. PicoBlaze SDK software interface is presented in figure 2.

This interface allow to software developer to edit and update firmware for each PicoBlaze microcontroller integrated in project. In order to use this application are necessary a few steps:

Select the workspace, or hardware project location. Application scan the chosen directory and find Xilinx ISE project file, and also check if additionally files are required for PicoBlaze functionality, like assembler or memory VHDL models files. Missing files are automatically generated in project directory.

Second step involves selection of project file. ISE project file is examined and application identifies all PicoBlaze microcontrollers and their own memory integrated in it. All of this information's are displayed in right window.

Next step involves selection of source file for one microcontroller which needs to be edited.

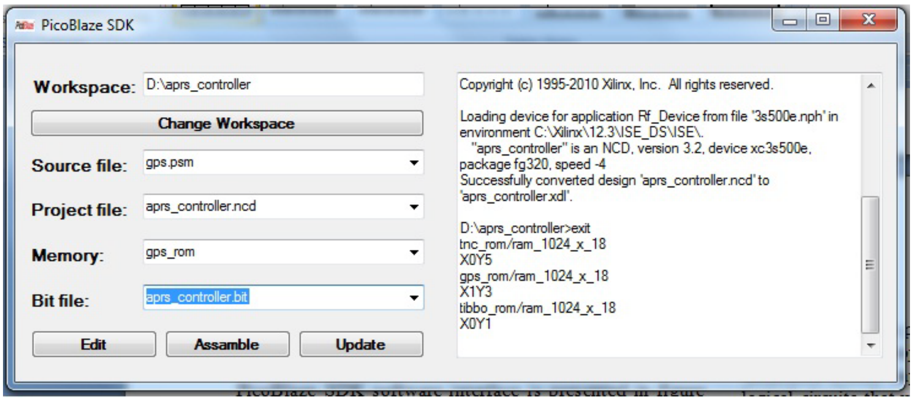
Next step involves selection of one PicoBlaze program memory, which will be updated with new program generated from selected source file.

One important step is to choose the bit file needed for hardware implementation in FPGA.

Program source file can be edited or modified by pressing the "EDIT" button. A text editor program will open the source file.

After all modification are finished and saved, program can be assembled by pressing "Assemble" button. In right window, user can see if the assemble process is successfully finished or the source code has errors. In case of error, source file it can be modify by pressing the "EDIT" button again.

Update of hardware platform process can be started by pressing the "UPDATE" button.



Workspace: D:\aprs_controller

Source file: gps.psm

Project file: aprs_controller.ncd

Memory: gps_rom

Bit file: aprs_controller.bit

```
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Loading device for application Rf_Device from file '3s500e.nph' in
environment C:\Xilinx\12.3\ISE_DS\ISE\.
   "aprs_controller" is an NCD, version 3.2, device xc3s500e,
package fg320, speed -4
Successfully converted design 'aprs_controller.ncd' to
'aprs_controller.xdl'.

D:\aprs_controller>exit
tnc_rom/ram_1024_x_18
X0Y5
gps_rom/ram_1024_x_18
X1Y3
tibbo_rom/ram_1024_x_18
X0Y1
```

Figure 2. PicoBlaze SDK software interface

III. EXPERIMENTAL RESULTS

Experimental platform, which is presented in figure 3, is developed by using Spartan 3E Starter Board, GPS receiver, TNC for radio station interface and TIBBO LAN module. Software development for each PicoBlaze microprocessor it was made by using PicoBlaze SDK tool.

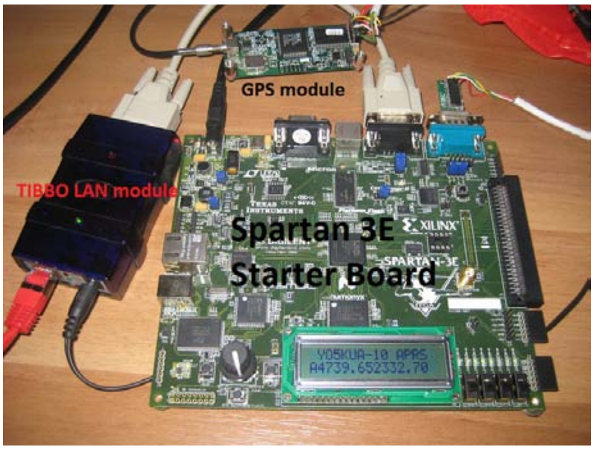


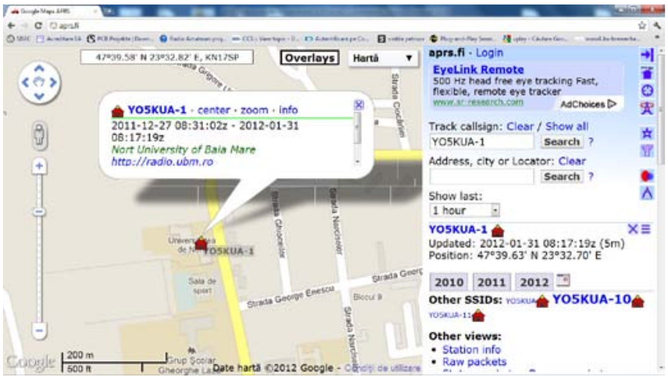
Figure 3. Experimental platform

Data from GPS module and filtered data from TNC terminal are routed to internet connection.

The Lassen SK II GPS is a tracking GPS receiver designed to operate in L1 frequency, Standard Position Service, Coarse Acquisition code. The receiver is designed in a modular format, suited for embedded applications. I use two highly integrated Trimble custom integrated circuits. The Lassen SK II GPS features the latest signal processing application, a high-gain RF section suitable for standard 25 dB active gain GPS antennas, and a CMOS TTL level pulse-per-second (PPS) output for timing applications or as a general purpose synchronization signal.

The Lassen SK II GPS operates using either of three protocols — Trimble Standard Interface Protocol (TSIP), Trimble ASCII Interface Protocol (TAIP), and NMEA 0183. The Lassen SK II GPS also supports RTCM SC-104 for DGPS. [4, 10]

In figure 4 and 5 are presented maps positioning of APRS node controller implemented and presented in this paper.


47°39.58' N 23°32.82' E, KN17SP

YO5KUA-1 · center · zoom · info
2011-12-27 08:31:02z - 2012-01-31 08:17:19z
Nort University of Baia Mare
http://radio.ubm.ro

aprs.fi · Login

EyeLink Remote
500 Hz head free eye tracking Fast, flexible, remote eye tracker
www.sr-research.com

Track callsign: Clear / Show all
YO5KUA-1

Address, city or Locator: Clear

Show last:
1 hour

YO5KUA-1
Updated: 2012-01-31 08:17:19z (5m)
Position: 47°39.63' N 23°32.70' E

Other SSIDs: YO5KUA YO5KUA-10 YO5KUA-11

Other views:
- Station info
- Raw packets

Figure 4. Map position using I-Gate function

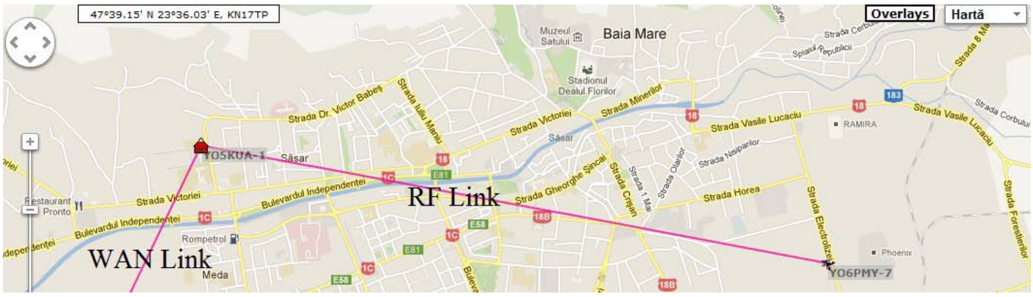


Figure 5. Map position using TNC function

IV. CONCLUSIONS

The SDK application is developed by paper author, and offer good software tool for PicoBlaze microcontroller applications. It can be used in teaching process, allowing the student to focus on PicoBlaze firmware development not on implementation of project.

Application presented and performed, is a component within a wider project, which proposes the creation of a dedicated system implemented with intelligent programmable logical circuits that will apply in wireless sensors networks.

Further development of the project involves adding new functionality, possibility to choose the type of PicoBlaze microcontroller, suitable for implementation on Spartan2 or Spartan6 FPGA chip, implementation of an algorithm for transmission of data from ZigBee wireless sensors networks.

Using the onboard LAN chipset provided by Spartan 3E Starter Board it's another stage of project development.

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